REMARKS

Claims 1-3, 5-7, and 9 were rejected for anticipation in view of Marko. Claims 4 and 8 were rejected as unpatentable over Marko in view of Carlson. Claim 10 was rejected as being unpatentable over Marko in view of Ishizu. Claim 11 was rejected as being unpatentable over Marko in view Ishizu in view of Downey. Applicant requests reconsideration. Independent claims 1 and 10 were amended to recite that the lead and lag signals are generated within a window period of time referenced to the adjusted timing pulses.

Ishizu and the prior art teach that a comparator can be used to detect zero crossings. Downey and the prior art teach that various modulation methods can be used to generate self-clocking baseband signal waveforms encoding a digital bit stream. Carlson and the prior art teach that windows can be used to count transitions therein and that that count can be compared to a predetermined value. The use of zero crossings, modulation methods, windows, and counters are all well known in the art. Ishizu, Carlson, and Downey teach well-known prior art components. However, none of these references teach lead and lag detection of transitions over a window period. The present invention enables more precise timing and faster tracking of the timing of a baseband signal encoding a digital bit stream.

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Marko teaches an accumulator for adjusting a clocking signal as part of a timing recovery loop. However, Marko does not anticipate because Marko uses phase detection, which teaches away from the present invention as strong evidence of nonobviousness. The combination of Marko with Ishizu, Carlson, and Downey does not reach the claimed invention. In Marko there is a recovery time loop that is designated by items 902, 904, 906, 908, 910, 916, 926, 932 shown in detail in Figure 9A. In the present inventions, the timing recovery loop includes items 10, 12, 16, 18, 20, 22, 26, 14, and 11. These two loops particularly differ in that Marko generates early and late signals based upon phase detection, whereas, the present invention generates lead and lag signals based upon window detection. Both Marko at 902 and the present invention at 10 have a baseband signal input encoding a digital bit stream. Both Marko at 992 and the present invention at 15 provide a digital bit stream output. The objects are the same. Of course, the fundamental difference is how adjustments are made to the clocking signal for precisely detecting the digital bit stream.

The primary object of a timing recovery loop is to provide a timing signal that can be used to clock a baseband signal encoding a digital data stream into that digital data stream. The original baseband signal is self-clocking in that it contains transitions, high to low, and low to high, that define bit periods and that can be used to generate and adjusting the clocking signal for tracking the timing of the baseband signal having early and late baseband transitions.

In the present invention, a baseband waveform 10 is clocked using a data detector 11 to generate adjusted timing pulses 14 used to generate the digital bit stream 15. In Marko, at Figure 5, the designated as prior art includes a recovered clock 502, which is a baseband clock signal, includes recovered data 504, which is a baseband signal encoding the digital bit stream, and center bit sampled data 506, which is the desired digital bit stream. The "early transition" of the leading edge of BIT1 shows that the recovered data edges are early or late by a phase in reference to the recovered clock. In Figure 6 of Marko, the recovered clock signal 604 is compared with recovered data 606. The recovered clock refers to early and late transitions of the clock 604 relative to the recovered data 606 having late and early transitions.

Marko uses an early and late accumulator 912 for counting early and late signals 908. The accumulator counts early and late phase detections over an accumulation time. When accumulator counts to twenty, for example, meaning twenty more early transitions than late transitions, the clock timing is adjusted and the accumulator is cleared. Thus, the accumulation time is not fixed but variable depending on rates of early and late phase detections. The sign indicates whether there are more early detections or more late detections. The accumulator sign is used to then adjust the clocking signal in increments of 1/32 of a bit period, being the phase detection period.

Marko uses a sign signal 914, a frequency offset correction circuit 916, a multiplexer 926, a reference clock 934, and a

divider 932 for generating a narrow BW recovered clock. The present invention uses a count magnitude generator 18, a count sign clipper 20, a threshold comparator 22, a timing pulse delay adjustor 26, reference timing pulses 26, and a timing pulse delay 34 for generating adjusted timing pulses 14. While the specific means are difference, both Marko and present invention provide timing signals used to clock the baseband signal encoding the digital bit stream for generating the digital bit streams. However, the benefit of the present invention lies in the new way of adjusting the timing signals derived from the original baseband signal. This difference is made clear by understanding the difference in function between Marko's phase detector 906 and applicant's comparator 12.

Marko's phase detector generates early and late signals respectively indicating when baseband transitions are early or late relative to the clocking signal. When the clocking signal transitions are early or late by at least that phase amount of time, with is 1/32 of a bit period, early and late phase detections are accumulated to a predetermined count when the clocking signal is adjusted. The clocking signal transitions are early or late relative to baseband detected transitions when early or late by a predetermined bit period phase amount, which is a fraction of a bit period amount of time as a clock phase. Hence, Marko uses a phase detector, for example, by a 1/32 phase of a bit period. The early and late accumulations can randomly walk indefinitely without adjusting the clocking signal as long as early and late detections do not exceed a predetermined amount of the early or late phase detections as accumulated by the accumulator. As such, Marko

teaches transition phase detection, in fractional bit period phases, for each bit period, for generating early and late signals, for each bit period, accumulated over an indefinite number of bit periods of time, for adjusting the clocking signal by that fractional bit period.

The present invention uses a random walk counter 16 for counting +1 lead and -1 lag signals derived from transitions occurring within a window period of time. The lead and lag signal are accumulated. When the accumulated number early or lag signals reaches a threshold value, the adjusted timing pulses are adjusted. The accumulation of leads and lags is over a plurality of bit periods. Significantly, the present invention determines lead or lag transitions using a window period of time, so that, regardless of how small is the early or late baseband transitions to the adjusted clocking signal, there may be a lead or lag, as nothing is really perfect. That is, even under very accurate perfect timing, the window can be used for generating lag and lead signals, which is not limited by how much time in bit period phase are the transitions early or late relative to the adjusting timing pulses, such as by phase detection in Marko.

The window may be a 1/2 of a bit period, one bit period, or a plurality of bit periods. However, the lead and lag signals are generated over a window time period. The window time size can vary, but preferably is less that one bit period. However, as soon as a lead or lag signal is detected within the window, the counter 16 is immediately updated, and the adjusted timing pulse can be

immediately adjusted depending on the threshold value. This provides for adjusting the adjusted timing pulses even when the transitions are early or late less than a predetermine amount of time corresponding to a bit period phase as detected in Marko.

The present invention teaches lead, none, and lag signal detection by comparison over a window period of time with the lead and lag signals being accumulated over a plurality of bit periods for adjusted the adjusted timing pulses. Marko teaches transition phase detection, in fractional bit period phases, for each bit period, for generating respective early and late signals, for each bit period, accumulated over an plurality of bit periods of time to a predetermined maximum value, for adjusting the clocking signal by that fractional bit period. Marko relies upon phase detection of early and late transitions for accumulating phase errors over a plurality of bit periods. The present invention relies on window transition comparison of early and late transitions as lead and lag signals accumulated over a plurality of bit period of time to a predetermined threshold value, for adjusting the clocking signal. This difference is significant. In Marko, the minimum timing error is the phase amount, which is preferably stated as 1/32 bit period, and the accumulator count, which is preferably stated twenty, both of which mean that 1/32 bit period error is multiplied by the twenty accumulator count for providing a total error accumulation of 20/32 of a bit period. This is large, imprecise, and slowly reached. Marko must have at least this amount of error before an adjustment will be made.

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In Marko, the transitions must be off-center at least a phase amount of time. This phase amount of time is a minimum error amount required before any adjustment in the accumulator, which must count up before adjusting the clock signal. When the transitions are off less than that this phase amount of time, no early and late signals are generated, and no accumulation occurs, and no timing adjustment is made, yet, even smaller offsets in transition phase can degrade the clock timing over time, and hence, degrade data detection. However, when transitions are determined to be leads or lag, by virtue of merely within a window period of time, as in the present invention, then each transition may cause a lead or lag signal, particularly even when the transition error offsets are less than Marko's phase. As such, the present invention will start the accumulation of "apparent" timing error offsets and will then adjust the adjusted timing pulses, even when the transition error offsets are practically insignificant when much less than Marko's phase error. The present invention preferably uses baseband zero crossing detections, which tend to be noisy detection when zero crossing. However, the undesirable use of zero crossings producing false or redundant transitions, and, the generation of an excessive number of lead and lag signals, one for every window even when near perfectly aligned, become insignificant, because the lead and lag signal are generated regardless of the amount of phase offset thereby providing canceling lead and lag signals during accumulation. In effect, the present invention quickly and accurately servos into perfect timing, despite noisy zero crossings and despite an excessive number of lead and lag signal detections, whereas, Marko adjusts the timing only when a large phase offset is

detected and repetitively detected as accumulated over many bit periods, and as such, Marko's does not adjust for insignificant timing errors and does not adjust unless significant errors are detected over many bit periods. The present detects for de minimus errors, and hence, does not need to accumulate large errors over many bit periods. Because the lead and lag signals tend to equal each other over time, accumulated lead and lag signals in near perfect time alignment would not cause excessive adjustments over time, but can adjust when very small errors occurs over a few bit periods. The window comparison feature to generate lead and lag signals allows for more precise timing and much faster timing tracking that is well suited for multipath fading problems. Marko's system does not generate lead and lag signals over a window time and does not generate transition pulses from zero crossings.

Marko teaches that the recovered data boundaries are in 1/32 increments. As such, the transitions are not perfectly aligned in time and timed to the baseband waveform signal, but rather, are closely timed within 1/32 of the bit duration. The recovered data signal and a recovered clock signal are phase detected for generating early and late events that are accumulated. In determining the early and late events, transitions of the recovered clock are compared to transitions of recovered data. That is, two digital streams are phase compared using respective transitions. The recovery clock is used to sample the recovered data signal for determining the data bit stream. When the accumulation of early or late events occur, the recovery clock is adjusted by a reference clock, so that, the recovery clock is more centered within a bit

duration of the recovered data so as to more precisely sample the recovered data in the bit center for precisely generating the data bit stream. The adjustment to the reference clock however is done by dividing by either 31 or 33. That is, the recovery clock is also adjusted by 1/32 duty cycle duration. The 1/32 bit boundaries of the recovered data signal is a major error to precise bit timing. The 1/32 duty cycle duration of the recovered clock is a minor error to precise bit timing.

Significantly, the present invention generates positive and negative transition pulses directly from the baseband waveform signal preferably as the baseband waveform signal crosses zero. The transition pulses are directly aligned in time to the transitions of the baseband waveform signal, and as such, the transition pulses are in fact synchronized to the baseband waveform signal. Because the transition pulses are precisely aligned in time to the baseband waveform signal and are thus synchronized to the baseband waveform signal, there is no major error associated with the use of the transition pulses relative to the baseband waveform.

These transition pulses detected as lead and lag signals within a window are accumulated and the lead and lag accumulations are immediately used to adjust the adjusted timing pulses. As such, the present invention can adjust the adjusting timing pulses very quickly, within a few bit periods, whereas, Marko would take an indefinite amount of time, and at least the preferably 20 bit periods of 20 successive early or late signals. The present invention has a much faster response time, well suited for rapidly

changing environments, such as in the multipath fading environment where a receiver passes tall buildings down town causing the signal to move in time rapidly.

In the present invention, the transition pulses line up exactly with transition of the baseband signal for improved data detection. Marko's transitions are off as much as 1/32 of a bit period. When the transitions are off less that this phase period, no early and lag signals are generated. In the present invention, lead and lags are determined over a window period regardless of how much they are early or late, whereas, in Marko, the early and late signals are generated from a phase offset. The use of zero crossing detectors injects noise, but the counter is able to filter out toggling leads and lags as the sum is zero over time.

One skilled in the art would not use window detection, which may disadvantageously capture perfectly aligned transitions as erroneous lead and lag signals. One skilled in the art would not use zero crossings disadvantageously injecting noise and false detections into the lead and lag determinations. However, the benefit of such window detection and zero crossing detection enables rapid determination of a misalignment between baseband signal and the timing signal, regardless of how noisy the transitions are and how small is the offset from perfection is the time alignment. The invention would not have been obvious to anyone.

Marko's tracking loop uses early and phase detection and accumulation providing minor timing errors, major timing errors, and adjustment to the timing only when many phase time period are accumulated providing slow and imprecise timing. The present invention using lead and lag window detection and accumulation without the minor and major timing error and make adjustment in the presence of very small timing error over a few bit periods and hence is more precise and tracks much faster.

Marko does not, in anyway remotely suggest zero crossing transitions for generating lead and lag signals over a window period for determining when to adjust the clocking signal. The present invention, with a suitably size window time, will determine that a transition leads or lag, regardless of by how much they are early or late. As such, the present invention more quickly generates multiple lead and lag signals for more quickly updating the counter, and to more quickly adjust the timing pulses. This case being in good condition for appeal or allowance, applicant requests allowance of claims.

Respectfully Submitted

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